WHAT IS CLAIMED IS:

1. A magnetic memory comprising:

a plurality of variable resistors arrayed as memory elements in a matrix;

a plurality of bit lines which each of is arranged on each row of the matrix and connected to one terminal of each variable resistors belonging to the same row;

a read circuit which detects resistance values of said variable resistors based on currents flowing through said bit lines; and

at least one load element arranged on said bit lines independently of said memory elements.

2. A memory according to claim 1, wherein each load element includes a resistor having the same structure as a structure of said variable resistor, a resistor having a structure different from the structure of said variable resistor, a current source, a diode, or a combination of the resistor, the current source, and the diode.

3. A memory according to claim 1, wherein each variable resistor includes a magnetoresistive element.

4. A memory according to claim 3, wherein a said magnetoresistive element is magnetized mainly

perpendicular to a film surface.

5. A memory according to claim 3, wherein said magnetoresistive element is magnetized mainly parallel to a film surface.

6. A memory according to claim 1, further comprising a plurality of switches connected in correspondence with said variable resistors.

7. A memory according to claim 6, wherein each switch includes a field effect type transistor, a bipolar transistor, a thin film transistor, a diode, or a combination of the field effect type transistor, the bipolar transistor, the thin film transistor, and the diode.

8. A method of driving a magnetic memory which has a plurality of variable resistors arrayed in a matrix, a plurality of switches connected to the plurality of variable resistors, and a plurality of bit lines arranged on respective rows of the matrix, one terminal of each variable resistor being connected to a corresponding bit line, and the other terminal being connected to a corresponding switch, comprising the steps of:

suppressing variations in voltages of the bit lines;

applying a predetermined voltage to the variable resistors; and

detecting information written in the variable resistors based on currents flowing through the variable resistors.

9. A method according to claim 8, wherein in the step of suppressing variations in the voltages of the bit lines, one of the plurality of switches connected to the same bit line is always turned on.

10. A method according to claim 8, wherein in the step of suppressing variations in the voltages of the bit lines, one of the plurality of variable resistors connected to the same bit line is always selected.

11. A method according to claim 8, wherein in the step of suppressing variations in the voltages of the bit lines, a current is flowed to load elements arranged on the respective bit lines.